Claims

What is claimed is:

1. A gallium nitride (GaN) epitaxial structure manufactured in a growth chamber by a process comprising:

a) depositing one or more structural epitaxial layers on a substrate, the one or more structural epitaxial layers including a GaN buffer layer in the growth chamber; and

b) depositing a passivation layer on the one or more structural epitaxial layers, thereby forming a GaN structure that is passivated before the GaN structure is removed from the growth chamber.

2. The structure of claim 1 wherein the passivation layer is a thermally assisted silicon nitride passivation layer.

3. The structure of claim 1 wherein the depositing the one or more structural epitaxial layers comprises depositing a transitional layer on the substrate.

4. The structure of claim 3 wherein the depositing the one or more structural epitaxial layers further comprises depositing the GaN buffer layer on the transitional layer.

5. The structure of claim 4 wherein the depositing the one or more structural epitaxial layers further comprises depositing an aluminum gallium nitride (AlGaN) Schottky layer on the GaN buffer layer.

6. The structure of claim 5 wherein the depositing the one or more structural epitaxial layers further comprises depositing a GaN termination layer on the AlGaN Schottky layer.

7. The structure of claim 3 wherein the depositing the one or more structural epitaxial layers further comprises depositing a sub-buffer layer on the transitional layer.

8. The structure of claim 7 wherein the sub-buffer layer is essentially aluminum nitride.

9. The structure of claim 7 wherein the depositing the one or more structural epitaxial layers further comprises depositing the GaN buffer layer on the sub-buffer layer.

10. The structure of claim 9 wherein the depositing the one or more structural epitaxial layers further comprises depositing a aluminum gallium nitride (AlGaN) Schottky layer on the GaN buffer layer.

11. The structure of claim 10 wherein the depositing the one or more structural epitaxial layers further comprises depositing a GaN termination layer on the AlGaN Schottky layer.

12. The structure of claim 1 wherein the process further comprises:

a) forming a source contact on the one or more structural epitaxial layers in an etched source region of the passivation layer;

b) forming a gate contact on the one or more structural epitaxial layers in an etched gate region of the passivation layer; and

c) forming a drain contact on the one or more structural epitaxial layers in an etched drain region of the passivation layer,

thereby forming a high electron mobility transistor.

13. The structure of claim 1 wherein the process further comprises:

a) forming a source contact on the one or more structural epitaxial layers in an etched source region of the passivation layer;

b) forming a gate contact on the passivation layer; and

c) forming a drain contact on the one or more structural epitaxial layers in an etched drain region of the passivation layer,

thereby forming a metal-insulator-semiconductor field effect transistor.

14. A method of growing a gallium nitride (GaN) epitaxial structure comprising:

a) depositing one or more structural epitaxial layers including a GaN buffer layer on a substrate; and

b) depositing a thermally assisted silicon nitride passivation layer on the one or more structural epitaxial layers before the GaN epitaxial structure is removed from an associated growth chamber.

15. The structure of claim 14 wherein the depositing the passivation layer occurs immediately after the depositing the one or more structural epitaxial layers step while within the growth chamber.

16. The method of claim 14 wherein the depositing the passivation layer step is a thermally activated deposition process.

17. The method of claim 14 wherein the depositing the one or more structural epitaxial layers step comprises depositing a transitional layer on the substrate.

18. The method of claim 17 wherein the depositing the one or more structural epitaxial layers step further comprises depositing the GaN buffer layer on the transitional layer.

19. The method of claim 17 wherein the depositing the one or more structural epitaxial layers step further comprises depositing an aluminum gallium nitride (AlGaN) Schottky layer on the GaN buffer layer.

20. The method of claim 19 wherein the depositing the one or more structural epitaxial layers step further comprises depositing a GaN termination layer on the AlGaN Schottky layer.

21. The method of claim 17 wherein the depositing the one or more structural epitaxial layers step comprises depositing an aluminum nitride (AlN) sub-buffer layer on the transitional layer.

22. The method of claim 21 wherein the depositing the one or more structural epitaxial layers step further comprises depositing the GaN buffer layer on the sub-buffer layer.

23. The method of claim 22 wherein the depositing the one or more structural epitaxial layers step further comprises depositing an aluminum gallium nitride (AlGaN) Schottky layer on the GaN buffer layer.

24. The method of claim 23 wherein the depositing the one or more structural epitaxial layers step further comprises depositing a GaN termination layer on the AlGaN Schottky layer.

25. The method of claim 14 further comprising:

a) etching a source, gate, and drain regions of the passivation layer;

b) forming a source contact on the one or more structural epitaxial layers in the etched source region of the passivation layer;

c) forming a gate contact on the one or more structural epitaxial layers in the etched gate region of the passivation layer; and

d) forming a drain contact on the one or more structural epitaxial layers in the etched drain region of the passivation layer,

thereby forming a high electron mobility transistor.

26. The structure of claim 25 wherein the first, second, and third regions of the passivation layer are etched using a wet chemical etch.

27. The structure of claim 25 wherein the first and third regions are etched using a wet chemical etch and the second region is etched using a dry chemical etch.

28. The method of claim 14 further comprising:

a) etching a source and drain region of the passivation layer;

b) forming a source contact on the one or more structural epitaxial layers in the etched source region of the passivation layer;

c) forming a gate contact on the passivation layer; and

d) forming a drain contact on the one or more structural epitaxial layers in the etched drain region of the passivation layer,

thereby forming a metal-insulator-semiconductor field effect transistor.

29. The structure of claim 28 wherein the first and second regions of the passivation layer are etched using a wet chemical etch.